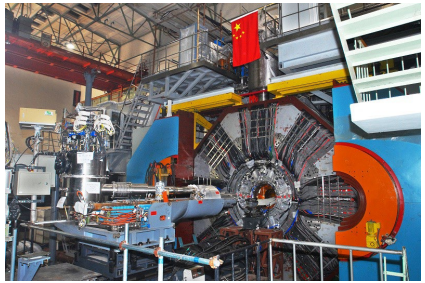
TECNOLOGIE AVANZATE

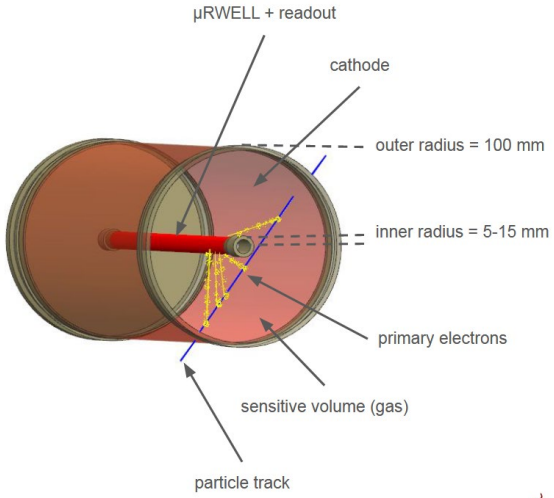
SISTEMI DI ACQUISIZIONE DATI E TEST BASATI SU FPGA

Michela Greco
michela.greco@unito.it

1W-WHO?



BESIII

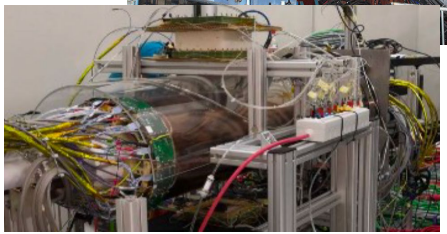


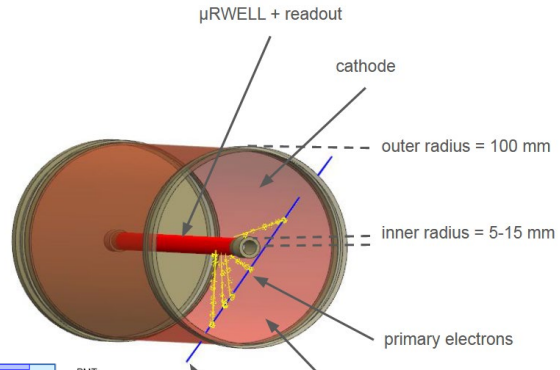
Tracking **R**ing **I**maging **C**heren**K**ov detector

μRtube

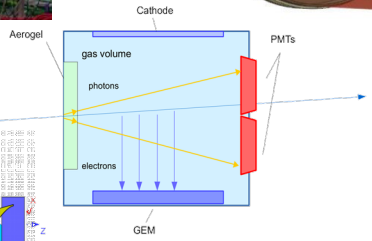
What Next
GIOVANI CHE RACCONTANO IL FUTURO

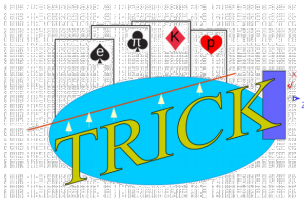
1W-WHAT?





μRtube





Tracking Ring Imaging CherenKov detector

BESIII

CGEM-IT
INFN-Fe, INFN-To, LNF

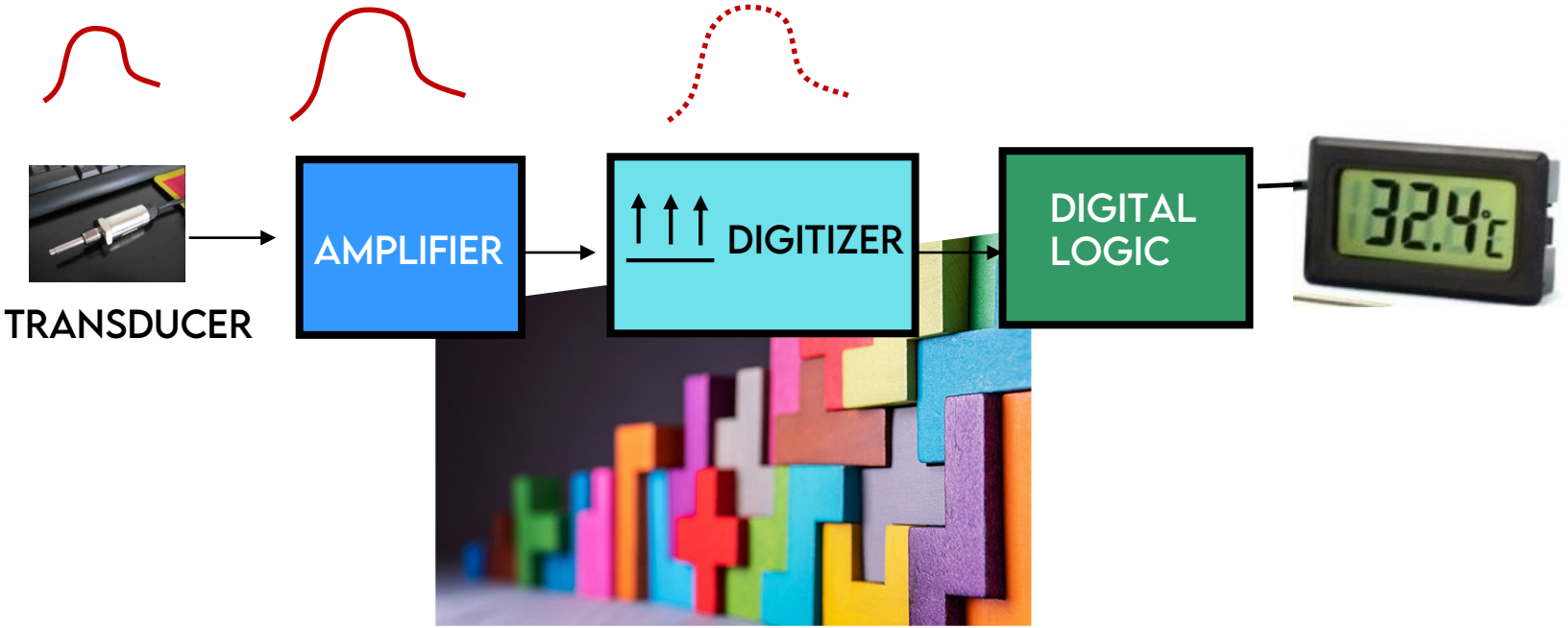
uRTube

Call Gruppo V, R. Farinelli
INFN-Fe,INFN-To
μRWELL tubolare

TRICK

Call Gruppo V, G. Mezzadri
MPGD+Cherenkov

2W-WHAT?

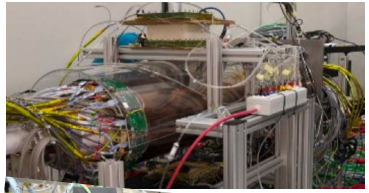


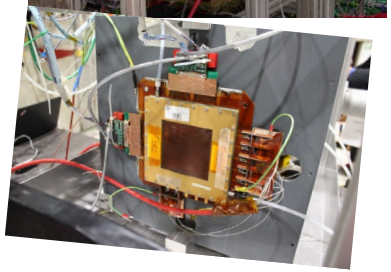
2W-WHAT?

TRANSDUCER

AMPLIFIER

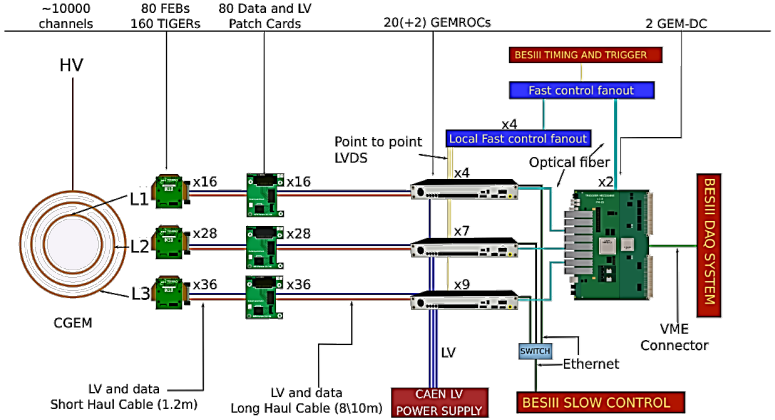
DIGITIZER





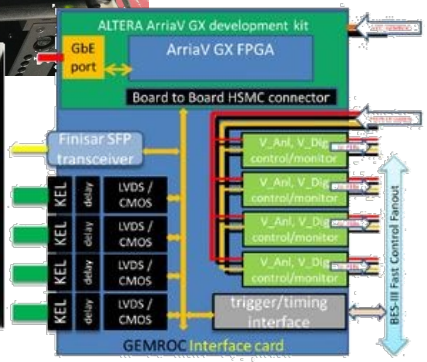
Bit Heart

>>PROF. RIVETTI, 6/4 H 18



2W-WHAT?

DIGITAL LOGIC

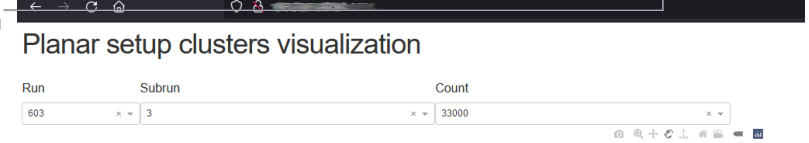


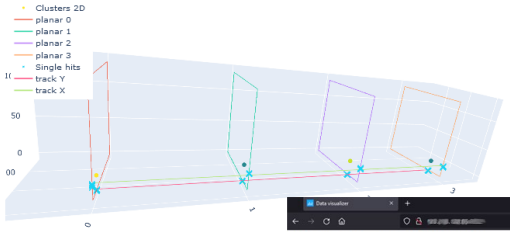
GUFI DAQ

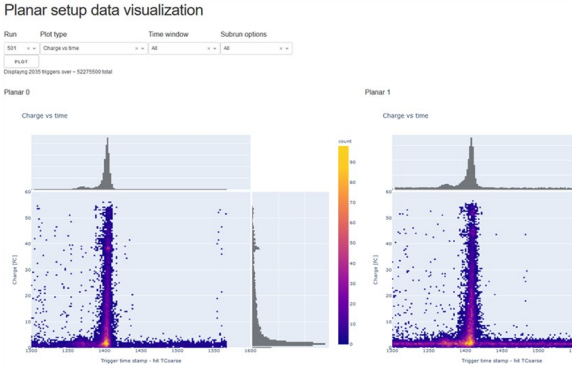
@A. Bortone

GUFI monitoring

Decode
Calibration
Clusterization
Tracking
Cluster Selection
Alignment



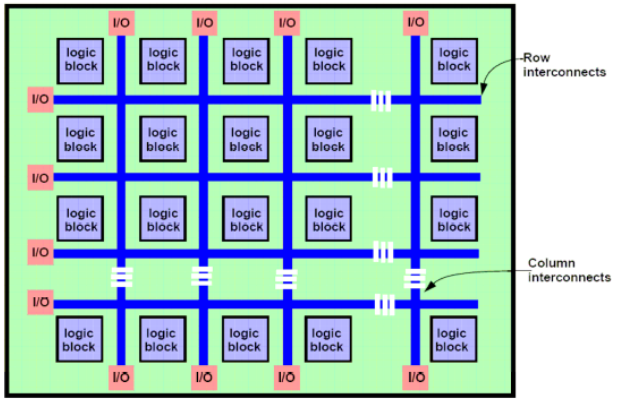


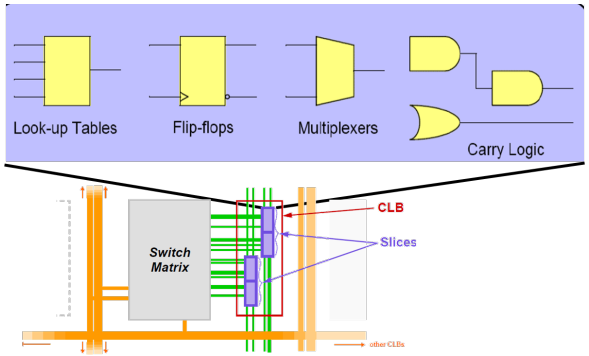


2W-
WHAT IS AN FPGA?
FIELD PROGRAMMABLE GATE ARRAY

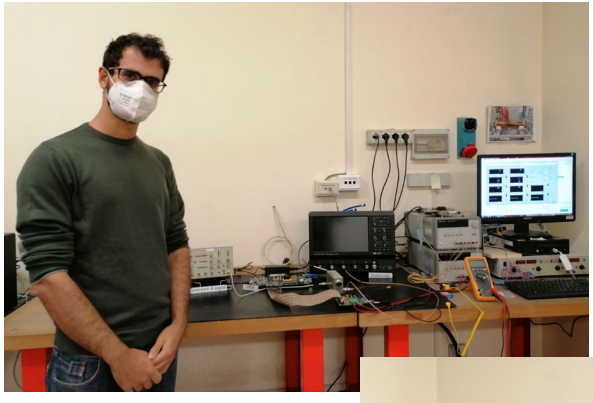
.. a very quick answer…

An FPGA is an integrated circuit
An FPGA is programmable in the field (=outside the factory)
Design is specified by schematics or with a hardware description language
Tools compute a programming file for the FPGA (gateware or firmware)
The FPGA is configured with the design
Your electronic circuit is ready to use!

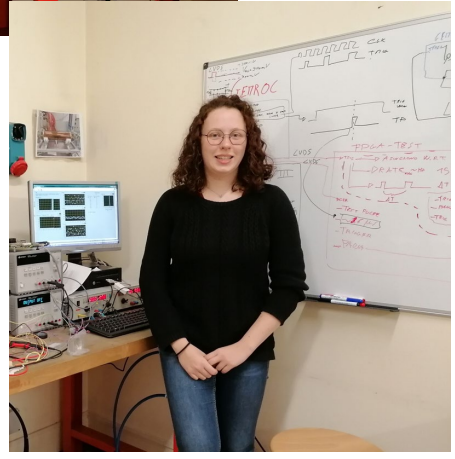


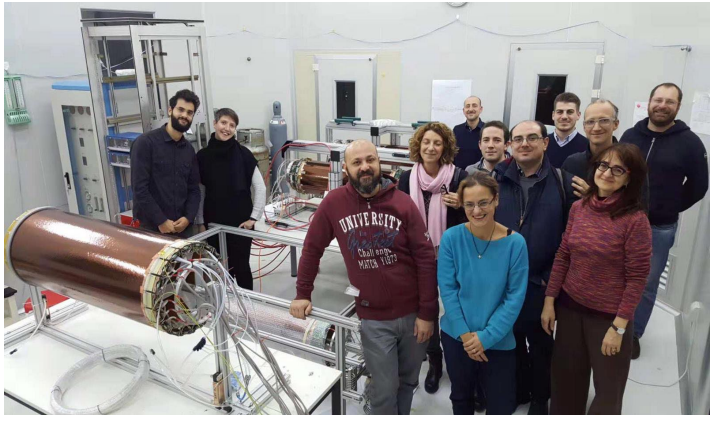


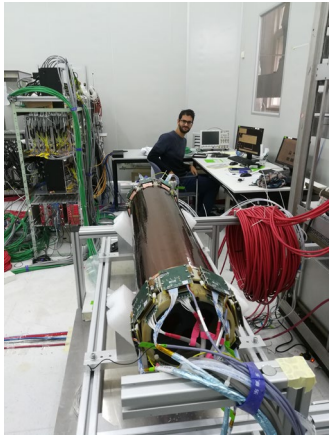
3W-WHERE?



LAB 3P NE







4W-WHEN?

BSc / MSc

BESIII

Analisi dati cosmici
Analisi dati TEST BEAM

BESIII-GEMROC 2.0

Migrazione a nuova FPGA e test
Implementazione di tool automatici per scansione stato e performance TIGER
Design e caratterizzazione di upgrade alle PCB
Adattamento del sistema di acquisizioni e analisi a nuovi progetti

uRTube

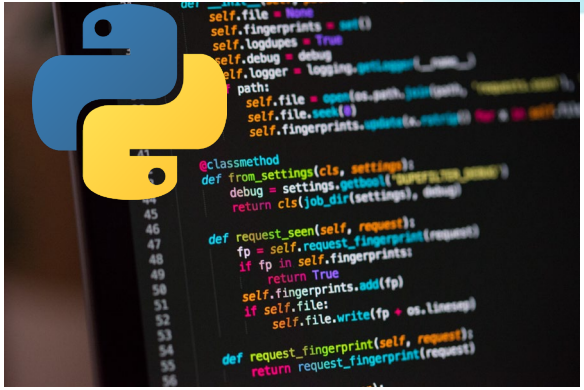
readout TIGER+GEMROC
misure di rumore ed ottimizzazione del piano di massa.
ricostruzione con il TIGER del signale µRtube simulato
misure dE/dx, dN/dx
presa dati sotto fascio

TRICK

Caratterizzazione con MA PMT
Test sotto fascio

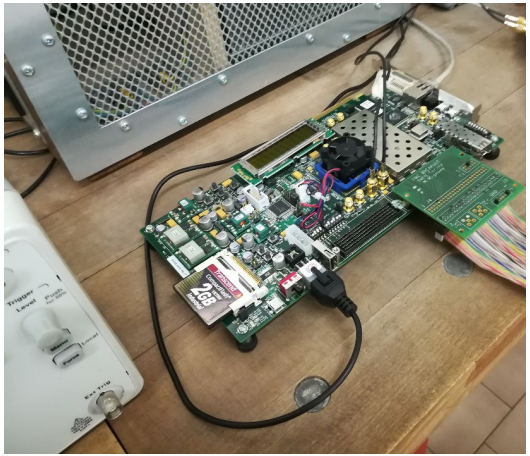
5W-WHY?

PYTHON



```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Contatore_LED_TB IS
END Contatore_LED_TB;

ARCHITECTURE behavior OF Contatore_LED_TB IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT Contatore_LED
    PORT(
         CLK : IN  std_logic;
         ENABLE : IN  std_logic;
         RESET : IN  std_logic;
         UP_DOWN : IN  std_logic;
         D2 : OUT  std_logic;
         D3 : OUT  std_logic;
         D9 : OUT  std_logic;
         D10 : OUT  std_logic);
    END COMPONENT;

   --Inputs
   signal CLK : std_logic := '0';
   signal ENABLE : std_logic := '0';
   signal RESET : std_logic := '0';
   signal UP_DOWN : std_logic := '0';

   --Outputs
   signal D2 : std_logic;
   signal D3 : std_logic;
   signal D9 : std_logic;
   signal D10 : std_logic;
```

VIVADO



LABVIEW

VERILOG
VHDL

GRAZIE!

DOMANDE ?

michela·greco@unito·it