



TECNOLOGIE AVANZATE

SISTEMI DI
ACQUISIZIONE DATI
E TEST BASATI SU FPGA

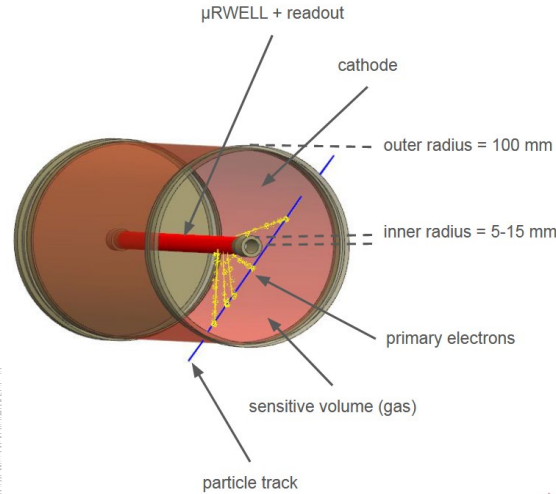


Michela Greco
michela.greco@unito.it

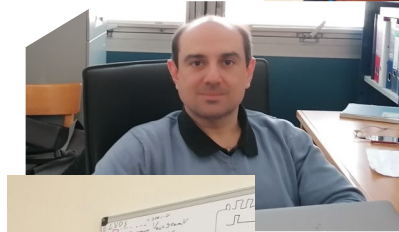
1W-WHO?



BESIII



μRtube



What
Next

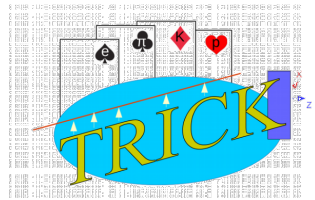
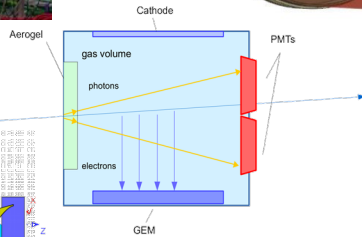
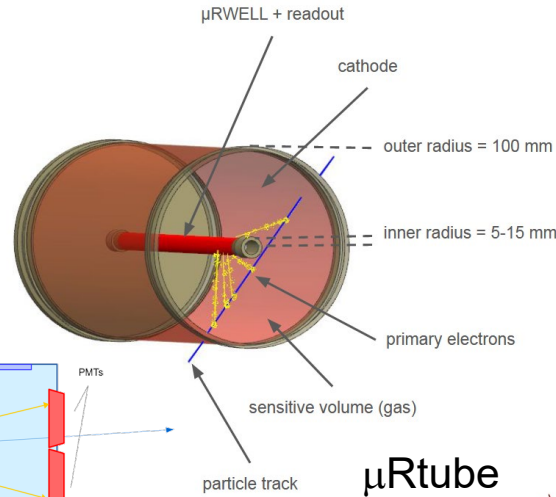
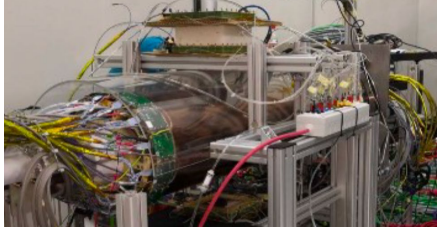
GIOVANI CHE RACCONTANO IL FUTURO

Tracking Ring Imaging CherenKov detector

1W-WHAT?



BESIII



BESIII

CGEM-IT
INFN-Fe, INFN-To, LNF

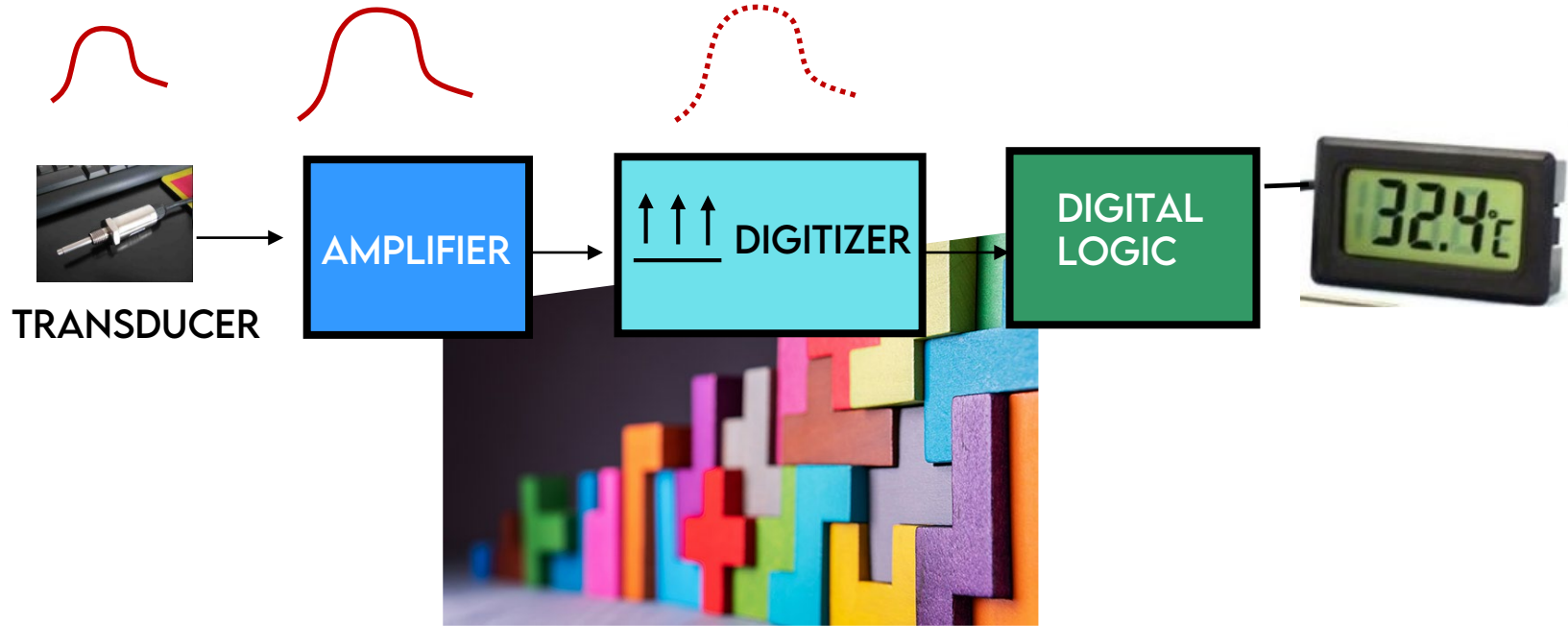
uRtube

Call Gruppo V, R. Farinelli
INFN-Fe, INFN-To
 μ RWELL tubolare

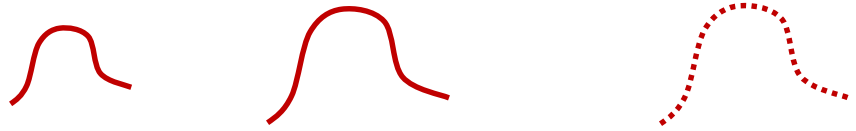
TRICK

Call Gruppo V, G. Mezzadri
MPGD+Cherenkov

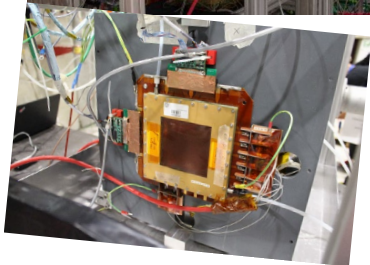
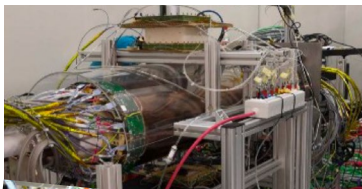
2W-WHAT?



2W-WHAT?

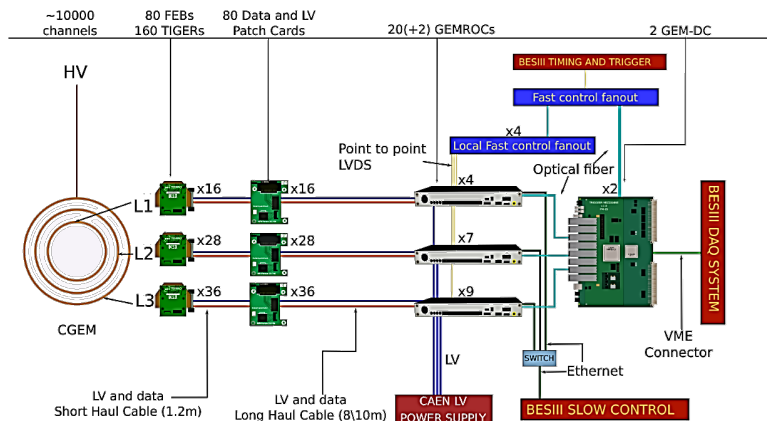


TRANSDUCER



Bit Heart

>>PROF. RIVETTI, 6/4 H 18



2W-WHAT?



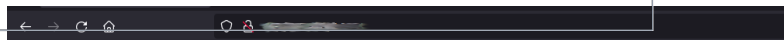
GUFU DAQ

@A. Bortone



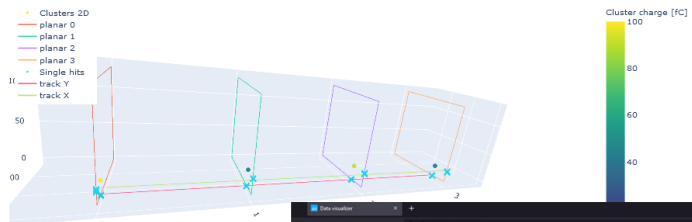
Decode
Calibration
Clusterization
Tracking
Cluster Selection
Alignment

GUFU monitoring



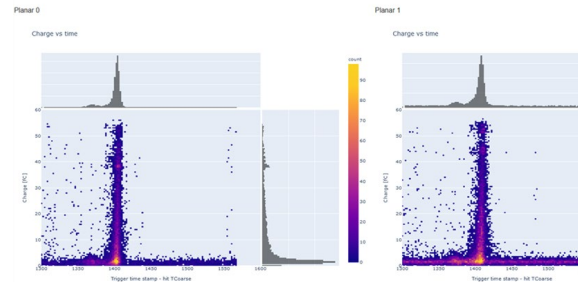
Planar setup clusters visualization

Run	Subrun	Count
603	3	33000

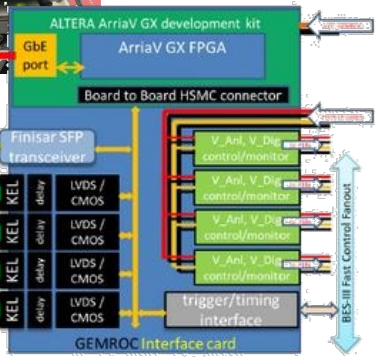


Planar setup data visualization

Run	Plot type	Time window	Subrun options
603	Charge vs time	All	All



DIGITAL LOGIC



2W- WHAT IS AN FPGA? FIELD PROGRAMMABLE GATE ARRAY

.. a very quick answer...

An FPGA is an integrated circuit

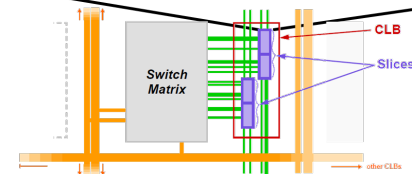
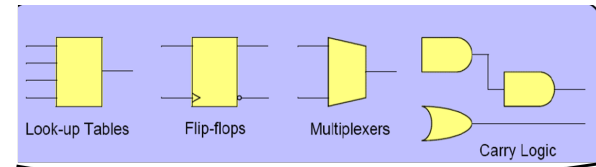
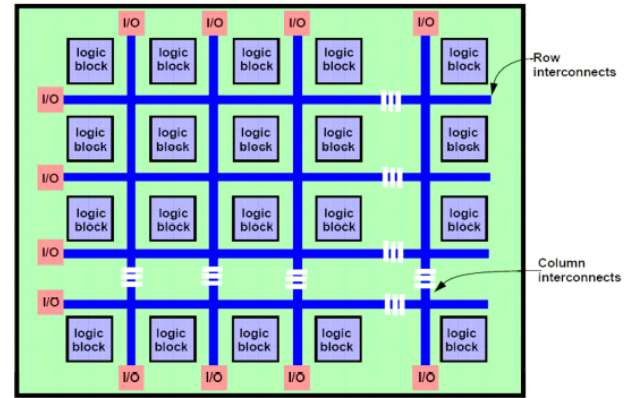
An FPGA is programmable in the field (=outside the factory)

Design is specified by schematics or with a hardware description language

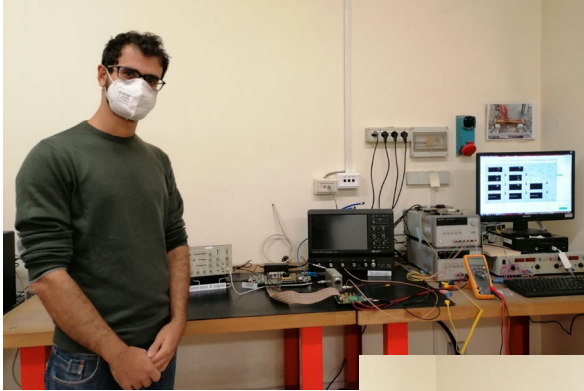
Tools compute a programming file for the FPGA (gateware or firmware)

The FPGA is configured with the design

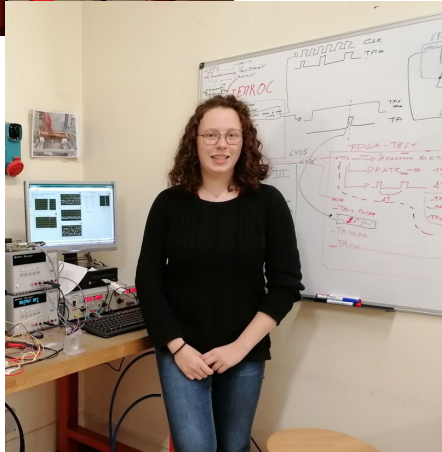
Your electronic circuit is ready to use!



3W-WHERE?



LAB 3P NE



4W-WHEN?

BSc / MSc

BESIII

Analisi dati cosmici
Analisi dati TEST BEAM

uRTube

readout TIGER+GEMROC
misure di rumore ed ottimizzazione del piano di massa.
ricostruzione con il TIGER del segnale μ Rtube simulato
misure dE/dx , dN/dx
presa dati sotto fascio

BESIII-GEMROC 2.0

Migrazione a nuova FPGA e test
Implementazione di tool automatici per scansione
stato e performance TIGER
Design e caratterizzazione di upgrade alle PCB
Adattamento del sistema di acquisizioni e analisi
a nuovi progetti

TRICK

Caratterizzazione con MA PMT
Test sotto fascio

5W-WHY?

PYTHON



```
self.file = None
self.fingerprints = set()
self.logdups = True
self.debug = debug
self.logger = logging.getLogger(__name__)
path:
self.file = open(os.path.join(path, "requests.txt"),
self.file.seek(0)
self.fingerprints.update(k.request) for k in self.req

@classmethod
def from_settings(cls, settings):
debug = settings.getboolean("debug", True)
return cls(job_dir(settings), debug)

def request_seen(self, request):
fp = self.request_fingerprint(request)
if fp in self.fingerprints:
return True
self.fingerprints.add(fp)
if self.file:
self.file.write(fp + os.linesep)

def request_fingerprint(self, request):
return request_fingerprint(request)
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Contatore_LED_TB IS
END Contatore_LED_TB;

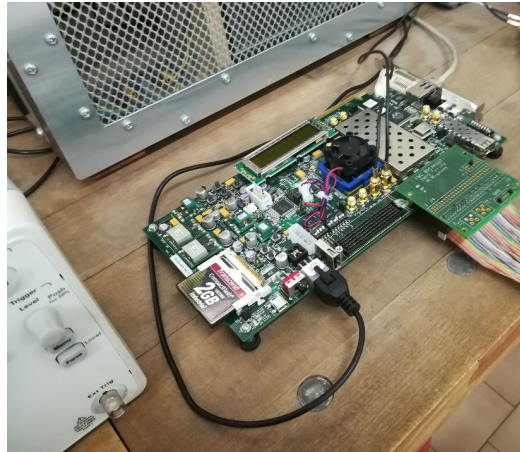
ARCHITECTURE behavior OF Contatore_LED_TB IS

-- Component Declaration for the Unit Under Test (UUT)
COMPONENT Contatore_LED
PORT (
CLK : IN std_logic;
ENABLE : IN std_logic;
RESET : IN std_logic;
UP_DOWN : IN std_logic;
D2 : OUT std_logic;
D3 : OUT std_logic;
D9 : OUT std_logic;
D10 : OUT std_logic;
END COMPONENT;

--Inputs
signal CLK : std_logic := '0';
signal ENABLE : std_logic := '0';
signal RESET : std_logic := '0';
signal UP_DOWN : std_logic := '0';

--Outputs
signal D2 : std_logic;
signal D3 : std_logic;
signal D9 : std_logic;
signal D10 : std_logic;
```

VIVADO



LABVIEW



VERILOG
VHDL



GRAZIE!

DOMANDE ?

Michela.Greco@unito.it